Performance Guarantees in Manycore Embedded Systems based on Network-on-Chip

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Abstract

Embedded applications have strict performance guarantees that must be met in every scenario. Such guarantees have to be verified – formally or empirically – at design time, and the verification process usually guides design space exploration towards configurations that can meet those guarantees at the lowest cost and lowest energy dissipation. Manycore systems pose new challenges to this process, as the exponential scaling of the number of possible system configurations makes it unlikely that an optimal configuration could be found. In this talk, a concrete manycore system architecture – namely Networks-on-Chip (NoCs) – will be used to illustrate the challenges of obtaining system configurations that are able to meet performance guarantees and requirements of real-time embedded applications.

The talk will be structured as follows. First, an introduction and motivation to communication-centric design of multi and manycore systems, followed by the basics of Networks-on-Chip architectures, with special emphasis to priority-preemptive virtual channels. Then, an overview of simulation and analytical models that can provide worst-case and average case NoC communication latency, as well as energy estimates, for application-specific communication load. Finally, an insight on how each of those models can be used as fitness functions in the design space exploration of NoC-based embedded systems, aiming to meet performance guarantees and optimise energy dissipation.